

**Reconfiguration Of VLSI Arrays By Covering  
(Technical Report. Texas A & M University. Computer  
Science Dept) By Fabrizio Lombardi**

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### **Dirk stroobandt | computer systems lab**

Computer Systems Lab (CSL) - HES (Hardware and Embedded Systems) team Electronics and Information Systems (ELIS) department Ghent University Sint Pietersnieuwstraat 41

### **On designing ulm-based fpga logic modules**

Department of Computer Sciences, University of Texas at Austin: Technical Report UCB/ERL M92/41, Dept. of Electrical Engg. and Computer Science,

### **Patent us7412586 - switch memory architectures -**

The present invention provides a switch memory architecture (SMA) consisting of: (i) processing elements (PE) (ii) memory banks (MB), and (iii) interconnect switches

### **Reconfiguration of vlsi arrays by covering - ieee**

In VLSI arrays, redundant cells are added as spares. The proposed approach is applicable as an offline technique at either production time and/or run time.

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### **Reconfiguration of vlsi arrays by covering (book,**

Reconfiguration of VLSI arrays by covering. [Fabrizio Lombardi; > # Reconfiguration of VLSI arrays by covering Texas A & M University. Computer Science Dept

### **Design, analysis and reconfiguration of**

U of I Only Design, analysis and reconfiguration of defect-tolerant VLSI and parallel processor arrays

### **Reconfiguration of high performance vlsi sub-**

Reconfigurable techniques attempt to realise maximum possible fault-free sub-arrays in mesh connected VLSI arrays with faulty elements. Although this problem has been

### **Patent us8471593 - logic cell array and bus system**

A logic cell array having a number of logic cells and a segmented bus system for logic cell communication, the bus system including different segment lines having

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388-391 2002 conf/ah/2002 AH db/conf/ah/ah2002.html#BraASS02 Maria A. M. Souto Regina Verdin

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## **Reconfiguration of vlsi arrays: a technique for**

The problem afforded is that of dynamic reconfiguration of regular arrays of processing elements, implemented as VLSI devices; the aim is that of achieving high

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2 Department of Computer Science and Electrical Engineering, Dept. of Electrical and Computer Engineering, M. Stankus. VSB - Technical University of Ostrava,

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## **Patent us8127061 - bus systems and reconfiguration**

A processor chip includes data processing elements that each has dedicated to it a respective switch for dynamically establishing an interconnection between the data

## **Pgroupw - user contributions [en]**

This cyberphysical domain provides unique challenges to many existing computer science algorithms, approaches and frameworks due to the data complexity,

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**Testing and reconfiguration of vlsi linear arrays**

Achieving fault tolerance through incorporation of redundancy and reconfiguration is quite common. In this paper we study the fault tolerance of linear arrays o

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Reader in Electronics and Computer Science, University of from Texas A&M University and his S.M from Istanbul Technical University,

**Advanced data layout optimization for multimedia**

Technical Report, University of Wisconsin, Lecture Notes In Computer Science The computational model considered is the arrays with a reconfigurable

**Efficient reconfiguration of vlsi arrays -**

We consider the problem of reconfiguring a 2-dimensional VLSI array with faulty cells. A network flow model of the problem is formulated and an algorithm is presented

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**Computer-aided design of integrated circuits and**

Lombardi, Fabrizio; In VLSI arrays, redundant cells are added as spares. Dept. of Computer Science. and Engineering. 354D IST Building.

**On the reconfiguration of degradable vlsi/wsi**

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**Patent us8230411 - method for interleaving a**

Patent US8230411 - Method for interleaving a program over a

**Citeseerx testing and reconfiguration of vlsi**

BibTeX @MISC{Prisco98testingand, author = {Roberto De Prisco and Angelo Monti and Linda Pagli}, title = {Testing and Reconfiguration of VLSI Linear Arrays}, year

## **Fault tolerance through reconfiguration in vlsi**

Fault Tolerance Through Reconfiguration in VLSI and WSI Arrays (Computer Systems Series)

Hardcover February 9, 1989

## **Www.worldcat.org**

integration 1988 Technical report ; 1988 en 18647828 18647828 Reconfiguration of VLSI arrays by covering Sami Texas A & M University. Computer Science Dept

## **Patent us8209653 - router - google patents**

Configuration of reconfigurable multidimensional fields are described. Information is provided for handling feedback, among other things.

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BibTeX-file{ %%% author = "Nelson H. F. Beebe", %%% version = "2.91

## **Patent us8156312 - processor chip for**

Patent US8156312 - Processor chip for reconfigurable data

## **Radzihovsky, leo - ml-struct-svm**

Texas AM University School Dept. of Physics Vanderbilt University, Dept. of Loughborough University ( Department of Computer Science and

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## **On the reconfiguration algorithm for**

In this paper, an improved algorithm is presented for the NP-complete problem of reconfiguring a two-dimensional degradable VLSI array under the row and column

## **Items in bibliography identified by a string**

Vanderbilt University .See of Cambridge Computer Laboratory Technical Report Technical Symposium on Computer Science

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